REMARKS

In paragraph 2, page 11 of the Final Action mailed June 5, 2003, the Examiner states that the "proposed drawing correction/and or the proposed substitute sheets of drawings filed on 19 May 1998 in the applicant's provisional U.S. Patent Application No. 60/086,153 have been disapproved because they introduce new matter into the drawings." The Applicant respectfully reminds the Examiner that provisional U.S. Patent Application No. 60/086,153 and the non-provisional U.S. Patent Application No 09/275,527 are separate and distinct applications. Accordingly, when the non-provisional U.S. Patent Application No. 09/275,527 was originally filed on 24 March 1999, no amendments to the drawings filed therewith were made. Therefore the Examiner's disapproval of the drawings based upon 37 CFR 1.121(a)(6) is unfounded.

At page 11, third paragraph of the Final Office Action, the Examiner states that incorporating by reference "Assignment Decision Diagram for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 was improper due to the belief of the Examiner that the cited reference was essential matter. The Applicant, however, still disagrees with the Examiner on this issue since the Chaiyakul reference is subject matter illustrating the state of the art (see MPEP 608.01(p)(A)) and therefore its incorporation by reference is a matter of convenience for the reader.

Also at page 12, first paragraph of the Final Office Action, the Examiner states that the "amendment to the specification, as compared to the priority document (provisional U.S. Patent Application No. 60/086,153 filed 24 March 1999[1]) is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure." The Applicant again respectfully reminds the Examiner that provisional U.S. Patent Application No. 60/086,153 and the non-provisional U.S. Patent Application No. 09/275,527 are separate and distinct applications and therefore a rejection under 35 U.S.C. 132 is improper. Since the applications are separate and distinct, the filing of the non-provisional U.S. Patent Application No. 09/275,527 on 24 March 1999 does not constitute adding new matter by amendment to the provisional application 60/086,153 and therefore cancellation of the new matter as requested by the Examiner is unwarranted.

All claims were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant believes that the specification of the non-provisional U.S.

Patent Application No. 09/275,52 properly provides support for all claims. The Examiner appears to be saying that the provisional U.S. Patent Application No. 60/086,153 does not provide support for claims 1 – 28 and therefore do not qualify for priority under 35 U.S.C. 119(e) and not, as recited in the Final Office Action, rejected as being unpatentable under 35 U.S.C. 112, first paragraph. Nonetheless, the Applicant believes that the provisional U.S. Patent Application No. 60/086,153 does provide sufficient support for claims 1 – 28 to qualify for priority under 35 U.S.C. 119(e) and that the non-provisional U.S. Patent Application No. 09/275,527 properly provides support for claims 1 - 28. In any case, all of the cited references pre-date the filing date (19 May 1998) of the provisional application 60/086,153 and any questions of priority under U.S.C. 119(e) are moot.

A number of claims were rejected under 35 U.S.C. 112, second paragraph in that the term "substantially" is ambiguous. Accordingly, the claims so rejected have been amended in accordance with the Examiner's rejection and thus renders the 35 U.S.C. 112, second paragraph moot.

Claims 1, 2, and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,632,418 issued to Rostoker et al (*Rostoker*) in view of "Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski (hereinafter *Chaiykul*) and further in view of U.S. Patent 5,920,711 issued to Seawrite et al (*Seawrite*). The *Rostoker* reference teaches a system for interactive design and simulation of an electronic circuit (at Abstract) which the Examiner admits at page 14 second paragraph does not disclose converting the hardware design code to an ADD nor does *Rostoker* disclose annotating the ADD (at page 14 last paragraph). In order to cure the admitted deficiencies in the primary reference *Rostoker*, the Examiner cited the secondary references *Chaiykul* and *Seawrite*, respectively.

The *Chaiyakul* reference merely provides a general description of the ADD and does not teach or reasonably suggest annotating the ADDs described with control nodes that provide a window into or control the state of the ADD at a particular point associated with the control node. The Examiner attempts to overcome this acknowledged (by the Examiner) deficiency by citing *Seawrite* which merely describes the use of a breakpoint (that only stops operation of a program when the program reaches a specified address). A breakpoint therefore is strictly limited to stopping a program at a particular address location and does not, unlike a control node, suggest providing **control of a state** of a simulation process at a point associated with a

[1] The Examiner appears to be citing the filing date of the non-provisional application of 24 March 1999 and not the filing date of the provisional application of 19 May 1998.

particular control node. Such control infers that that process flow itself can be modified as desired and not, as with a breakpoint, merely stops execution of the program at a specific address location. Such process flow modifications include stopping, conditional branching, suspending, etc. such that the control nodes provide a number of control, diagnostic, and evalution tools not even remotely possible using only a breakpoint. Unlike the breakpoints described in *Seawrite*, control nodes in the context of the invention can be used 1) to represent a conditional branch in a control flow, 2) to represent an assignment operation, 3) used as a place holder, or, if needed, 4) used to suspend execution.

Accordingly, the invention as recited in claim 1 requires,

> "annotating the ADD representation of the process block with one or more control nodes **suitable for setting of a state within the process block** wherein when a particular control node is encountered, a state within the process block associated with the control node can be directly observed thereby eliminating an atomic nature of the process block so as to provide a non-atomic analysis of the behavioral model."

Therefore, in contrast to the cited references, the invention as recited in claim 1 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. By annotation it is meant that selected portions of a particular ADD are associated with any of a number of control nodes which can be used to stop, start, view, etc. the state of the ADD at any selected point within the ADD as well as control a flow within the process block. Therefore, the control nodes afford the ability to **observe and set** the states within a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. By affording the ability to observe and control a state within a process block, the logic simulation provided by the invention is more easily debugged and provides a more detailed description of the process being simulated than is possible by any approach contemplated by the references taken singly or in any combination.

Accordingly, the Applicant believes that claim 1 is neither anticipated or rendered obvious by any of the cited references taken singly or in any combination and is therefore allowable.

In order to support a U.S.C. 103(a) rejection of a number of dependent claims, the Examiner cited U.S. Patent 6.421,808 issued to McGeer (*McGeer*) in order to overcome the Examiner's assertion that *Rostoker* does not disclose control nodes and process trees. In citing

McGeer, the Examiner specifically points to various figures and associated portions of the detailed description of *McGeer* to support the assertion that *McGeer* discloses control nodes as taught by the invention. In the context of the invention, a control node is used to control the flow through a process block, or more specifically described at page 19, first paragraph of the detailed description, a control node is "responsible for maintaining control flow through the simulator. By way of example, each control node includes a next pointer that is used by the simulator to point to a next process step in the simulation proces". However, the only discussion of controlling the flow through a process in *McGeer* is located at column 20, lines 4 – 23, "Flow Control Through Processes" in terms of an "if-then statement" and NOT as described in the context of the various figures and associated portions of the detailed description cited by the Examiner. One such example is the "control node" of FIG. 14 of *McGee* that is defined as, "Circuits that are generated by routine ControlNode (vertex_type) follow a standard I/O pin definition as shown in the following figure. These circuits are called the control nodes". These circuits, although referred to as control nodes, ***do not control*** the flow through the process nor a state of the process associated with the control node.

Independent claim 7 recites substantially the same limitations of claim 1 albeit as a behavioral model, provided on a machine readable medium and is therefore allowable for at least the reasons stated for independent claim 1.

All of the dependent claims 2 – 10 depend either directly or indirectly from independent claims 1 or 7 and are allowable for at least the reasons stated with regards to the independent claims. Therefore, none of the cited references, taken singly or in any combination render any of the dependent claims 2 – 10 as unpatentable under U.S.C. 103(a) and the Examiner is respectfully requested to withdraw his rejections thereof.

The Examiner rejected claims 11 – 26 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,937,190 issued to Gregory (hereinafter referred to as G1) in view of U.S. Patent 5,870,608 issued to Gregory (referred to as G2) further in view of Chaiykul and further in view of McGeer. The G1 reference teaches architecture and methods for hardware description language source level analysis and does not teach or even remotely suggest use of control nodes that both provide for flow control within the process block. The Examiner admits at page 24 last paragraph that the G1 reference does not expressly disclose annotating the assignment decision diagram with a plurality of control nodes and therefore relies upon the G2 reference. The G2 reference describes a data structure for representing a parse tree associated with a block of text that allows text associated with a particular parse node(s) to be displayed in a manner specified

by the parse node. Therefore, the G2 reference only provides a mechanism for displaying a parse tree, or portions thereof, associated with HDL text and does not suggest providing any form of a control mechanism for modifying a flow through the parse tree. For example, FIG. 6 of the G2 reference provides an overview that illustrates the overall process of using parse nodes to create electronic or software-based structures. As can be seen, HDL text 2000 is created by a user while at compile time, a parse tree 2002 is created having nodes that correspond to portions of the HDL text as well as, for example, to cells 2004-2016 within a netlist 2018 in addition to portions 2020, 2022, of a display image 2024 used to analyze the netlist. Therefore, any reference to "nodes" in the G2 reference are parse nodes that form the parse tree 2002 that, in turn, correspond to portions of the HDL text, for example. At no point, however, does G2 teach or remotely suggest using these parse nodes as any form of control nodes or any other such structure to control the flow within the parse tree 2002. Accordingly, the G2 reference neither teaches nor reasonably suggests the use of control nodes to maintain a control flow through an associated parse tree.

Independent claim 11 recites in part,

> "(f) annotating the assignment decision diagram (ADD) with a plurality of selected control nodes that are responsible for maintaining control flow through the simulator and are suitable for setting of a state within the process block, wherein when a particular control node is encountered, a state within the process block associated with the control node can be directly observed thereby substantially eliminating an atomic nature of the process block"

Therefore, in contrast to the cited references, the invention as recited in claim 11 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. Therefore, the control nodes afford the ability to observe as well as control the states **within** a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block or control the processes therein, the Applicant believes that claim 11 and its associated dependent claims 12 – 26 are allowable over the cited references taken singly or in any combination.

The Examiner rejected claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,848,236 issued to Dearth in view of U.S. Patent 5,937,190 issued to Gregory further in view of Chaiykul. *Dearth* simply teaches computer program product that specifies a method of compiling a simulation object used by a simulator to simulate the operation of a digital

circuit and does not teach or even remotely suggest use of control nodes to provide a non atomic view of a state within a particular process block nor the control of a the process within a process block. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block or control the process therein, the Applicant believes that claims 27 and 28 are allowable over the cited references taken singly or in any combination.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all pending claims are allowable. Should the Examiner believe that a further telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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